REMARKS

Claim Rejections Under 35 U.S.C. § 112

Claims 6, 16, 19 and 20 were rejected under 35 U.S.C. §112, first paragraph, as "failing to comply with the written description requirement." Applicant respectfully traverses this rejection.

The "dedicated bus" as claimed by Applicant is clearly shown in the drawings and implicitly described in the present specification. Figure 2 shows that the bus 212 between the SDRAM 204 and the flash memory 206 is not coupled to any other device. This bus 212 is thus dedicated to the SDRAM 204 and the flash memory 206. While the word "dedicated" is not used in the specification, the dedicated bus 212 is implicitly described in paragraph 16 of the specification where it is stated that data transfer is direct from the flash 206 to the SDRAM 204.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-3, 5, 11, 12, 15, 18 and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Baltz et al.* (U.S. Patent No. 6,058,474). Applicant respectfully traverses this rejection.

Applicant respectfully disagrees with the Examiner's definition that the word "directly" implies "without intervention." As clearly pointed out by the Examiner, it is still possible to have intervention with a direct transfer.

The Examiner stated that col. 7, lines 46 – 60, which describes Figure 8 of *Baltz et al.*, shows a direct transfer from the EPROM 671 to the internal program memory 23 and that this is without intervention. However, not only does the passage at col. 7, lines 46 – 60 clearly state that "DMA0 100 transfers 1024 32-bit words of data from external 8-bit ROM 671..." but Figure 8 also shows a dotted line from the DMA0 100 device to the bus 73 between the internal memory 23 and EPROM 671. This clearly shows, by the dotted line, and describes not only intervention but control of the transfer process by the DMA0 device 100 in transferring a predetermined quantity of data words.

Baltz et al. contains numerous other references to such intervention and control by the DMA device. For example, col. 1, lines 53 – 60 states in part that "direct memory access (DMA) circuitry which is operable to transfer data from an external source of data to the internal memory." This passage additionally states that the DMA initialization circuitry causes the DMA circuitry to transfer data.

The Examiner also appears to agree with the Applicant that the DMA process requires intervention and control by the DMA circuitry. The Examiner stated in the Office Action at paragraph 19, line 9, that "The DMA circuitry of Baltz *controls* [emphasis added] data transfer but does not intervene." While this is contradictory, it does indicate that the Examiner also agrees that the DMA circuitry exerts some control over the transfer process in *Baltz et al.*

Control of the data transfer process of *Baltz et al.* is synonymous with intervention. It may be possible to intervene in a process without controlling it (e.g., monitoring or buffering), however Applicant is unclear as to how it is possible to control a process without intervening in that process.

There is no control or intervention used in the transfer of data in the processing system of the present invention as claimed. Applicant's invention is to a transfer of data between non-volatile memory and volatile memory without intervention by another device.

There is clear support in the present specification and drawings for the use of "without intervention" as used in Applicant's claims. Paragraph 0018, line 1 of the present application states that "[t]he present invention allows the non-volatile memory contents to be directly loaded into the SDRAM without intervention by the processor." Additionally, Figure 2 shows that the bus 212 between the SDRAM 204 and the flash memory 206 is not coupled to any other device. This implicitly makes the bus 212 a dedicated bus and thus free from any intervention.

Therefore, *Baltz et al.* not only neither teaches nor suggests Applicant's invention as claimed, *Baltz et al.* actually teaches away from Applicant's invention. *Baltz et al.* teaches that some control/intervention is required to transfer data from one memory to another. As stated in the Background section of the present application, this is a problem that Applicant's invention fixes.

Claim Rejections Under 35 U.S.C. § 103

Claims 4, 6-9, 14, 16-19 were rejected under 35 U.S.C. § 103(a) as being anticipated over *Baltz et al.*, in view of *Harari et al.* (U.S. Patent No. 6,266,724). Claims 4, 6-9, 14, 16-19 were rejected under 35 U.S.C. § 103(a) as being anticipated over *Baltz et al.*, in view of Shin (U.S. Patent No. 6,735,669). Claims 4, 6-9, 14, 16-19 were rejected under 35 U.S.C. § 103(a) as being anticipated over *Baltz et al.*, in view of *Harari et al.* as applied to claims 6 and 19, and further in view of *Shin*. Applicant respectfully traverses this rejection.

Baltz et al. is the only cited art alleged to show transfer of data without intervention between a non-volatile memory and a volatile memory. Since it has been clearly shown above

that *Baltz et al.* teaches away from Applicant's claimed invention, the combination of *Baltz et al.* with *Harari et al.* and *Shin* cannot anticipate Applicant's invention as claimed.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this response.

Respectfully submitted,

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